UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,779	03/18/2004	Hirofumi Harada	S004-5242	8062

40627 7590 05/16/2006

ADAMS & WILKS
17 BATTERY PLACE
SUITE 1231
NEW YORK, NY 10004

EXAMINER	
DOAN, THERESA T	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

5) L

Office Action Summary	Application No.	Applicant(s)	
	10/803,779	HARADA, HIROFUMI	
	Examiner	Art Unit	
	Theresa T. Doan	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-5 and 7-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5 and 7-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The cancellation of claims 2 and 6 in paper filed on 02/21/06 is acknowledged.

Claim Objections

2. Claims 3-5 and 8-12 are objected to because of the following informalities:

In claim 3, line 1, "A vertical" should be changed to - - The vertical - -.

In claim 3, line 2, ";" after "claim 1" should be changed to -- , --.

In claim 4, line 1, "A vertical" should be changed to - - The vertical - -.

In claim 4, line 2, ";" after "claim 3" should be changed to -- , --.

In claim 5, line 1, "A vertical" should be changed to - - The vertical - -.

In claim 5, line 2, ";" after "claim 1" should be changed to -- , --.

In claim 8, line 1, "A vertical" should be changed to - - The vertical - -.

In claim 8, line 2, ";" after "claim 7" should be changed to -- , --.

In claim 9, line 1, "A vertical" should be changed to - - The vertical - -.

In claim 9, line 2, ";" after "claim 8" should be changed to -- , --.

In claim 10, line 1, "A vertical" should be changed to - - The vertical - -.

In claim 10, line 2, ";" after "claim 7" should be changed to -- , --.

In claim 11, line 1, "A vertical" should be changed to - - The vertical - -.

In claim 11, line 2, ";" after "claim 7" should be changed to -- , --.

In claim 12, line 1, "A vertical" should be changed to - - The vertical - -.

In claim 12, line 2, ";" after "claim 7" should be changed to -- , --.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3-5 and 7-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (APA) in view of Kocon et al. (U.S. Pat. 6,351,009).

Regarding claims 1, 7 and 10, APA (Fig. 2) discloses a vertical MOS transistor comprising: a semiconductor substrate 1 of a first conductivity type (see Specification, page 1, lines 10-11); an epitaxial growth layer 2 of the first conductivity type which is formed on the semiconductor substrate 1 (see Specification, page 1, lines 8-11); a body region 3 of a second conductivity type which is formed on the epitaxial growth layer 2

(see Specification, page 1, lines 14-17); a heavily doped body contact region 8 of the second conductivity type which is formed on a part of a surface of the second conductivity type body region 3 (see Specification, page 1, lines 18-21); a heavily doped source region 7 of the first conductivity type (see Specification, page 1, lines 18-20), which is formed on a part of the surface of the second conductivity type body region that is covered with the heavily doped body contact region 8 (see Fig. 2 labeled by the examiner below); a silicon trench 4 piercing the second conductivity type body region 3 and the first conductivity type source region 7 to reach an inner part of the first conductivity type epitaxial growth layer 2 (Specification, page 2, lines 6-8); a gate insulating film 5 formed along walls and bottom of the silicon trench 4 (Specification, page 2, line 8); a heavily doped polycrystalline silicon gate 6 buried in the silicon trench 4 while surrounded by the gate insulating film 5 (Specification, page 2, lines 8-10); an intermediate insulating film 9 formed on the polycrystalline silicon gate 6 in the silicon trench 4 to reach a surface the semiconductor substrate 1; a metallic source electrode 16 being in contact with the intermediate insulating film 9, the heavily doped source region 7, and the heavily doped body contact region 8; and a metallic drain electrode 16 connected to a rear surface of the semiconductor substrate 1 (see Fig. 2 labeled by the examiner below).

APA does not disclose a heavily doped polycrystalline silicon gate 6 buried in the silicon trench 4 to a level of the first conductivity type source region 7, and an insulator disposed on the sidewalls of the trench and above the gate.

However, Kocon (Fig. 2) teaches a MOS- gated device 200 having a gate material 210, which is recessed within the trench 207 to a level of the first conductivity type source region 206 to permit the inclusion of an intermediate insulating film 212 of sufficient thickness to provide gate isolation (column 3, lines 36-38), the intermediate insulating film 212 including insulator portions disposed on the sidewalls of the silicon trench 207 and above the silicon gate 210. Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the device structure of APA by forming the silicon gate buried in the silicon trench to a level of the source region and by forming the intermediate insulating film including insulator portions disposed on the sidewalls of the silicon trench and above the silicon gate because the forming of such gate structure and the forming of such intermediate insulating film would eliminate the surface area required for gate-source dielectric isolation and would reduce the device size, as taught by Kocon (column 3, lines 10-13).

Regarding claim 8, Kocon further teaches the forming of a metallic source electrode 215 (see Fig. 2D) having a generally planar surface disposed in contact with the intermediate insulating film 212, the heavily doped source region 206 and the heavily doped body contact region 204, the forming of such metallic source electrode would not require the need for a masking procedure to form contact openings (column 3, lines 30-35).

Regarding claim 9, APA (Fig. 1) further discloses a metallic drain electrode 16 connected to a second surface of the semiconductor substrate opposite to the first surface thereof.

Regarding claims 3 and 11, it would have been obvious to substitute silicon oxide with silicon nitride for the insulator of the intermediate insulating film 212 because both silicon oxide and silicon nitride are equivalent materials in using to form an isolation dielectric layer to isolate the gate material in trench.

Regarding claims 4-5 and 12, APA does not disclose that the heavily doped polycrystalline silicon gate buried in the silicon trench is 0.5 μm to 1.0 μm down from the top of the trench.

However, Kocon (Fig. 2) teaches a MOS- gated device 200 having a gate material 210, which is recessed within the trench 207 to permit the inclusion of an intermediate insulating film 212 of sufficient thickness to provide gate isolation (column 3, lines 36-38). In additional, Kocon teaches a typical minimum thickness of about 0.5 μm to 0.8 μm for dielectric layer 111 that imposes limitations on the minimum size of device 100 (see Fig. 1). It would be desirable to be able to reduce the size and improve the efficiency of semiconductor devices (column 2, lines 1-9). Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the device structure of APA by forming the heavily doped polycrystalline silicon gate buried in the silicon trench is 0.5 μm to 1.0 μm down from the top of the

trench would be able to reduce the size and improve the efficiency of semiconductor devices, as taught by Kocon (column 2, lines 1-9). Furthermore, it has been held that when the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation. In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

Response to Arguments

5. Applicant asserts that in this amendment, original independent claim 1 has been amended to incorporate the subject matter of allowable dependent claim 2. However, the indication of allowability of dependent claim 2 in the previous office action is withdrawn because of the new ground of rejection is applied.

Conclusion

This action is made non-final.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T. Doan whose telephone number is (571) 272-1704. The examiner can normally be reached on Monday to Friday from 7:00AM - 4:00PM.

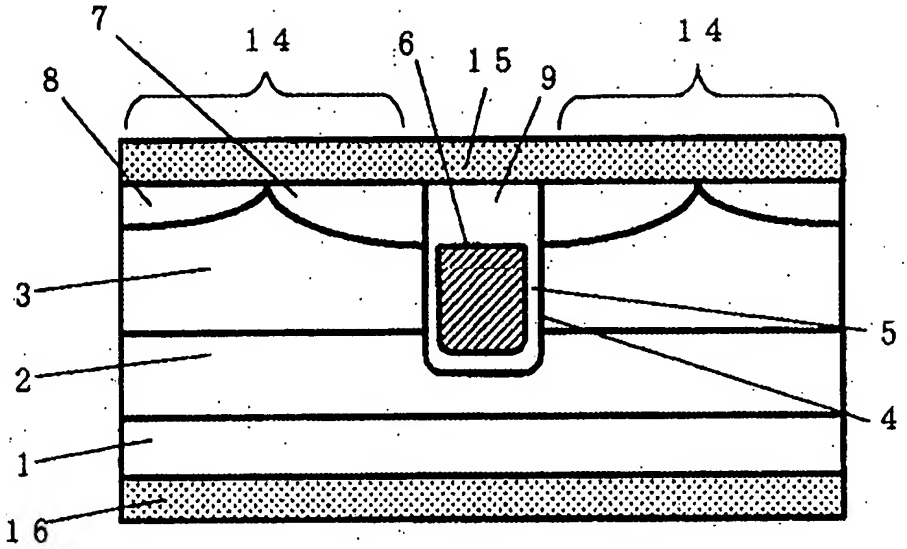
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Theresa Doan
May 11, 2006.

Replacement Sheet

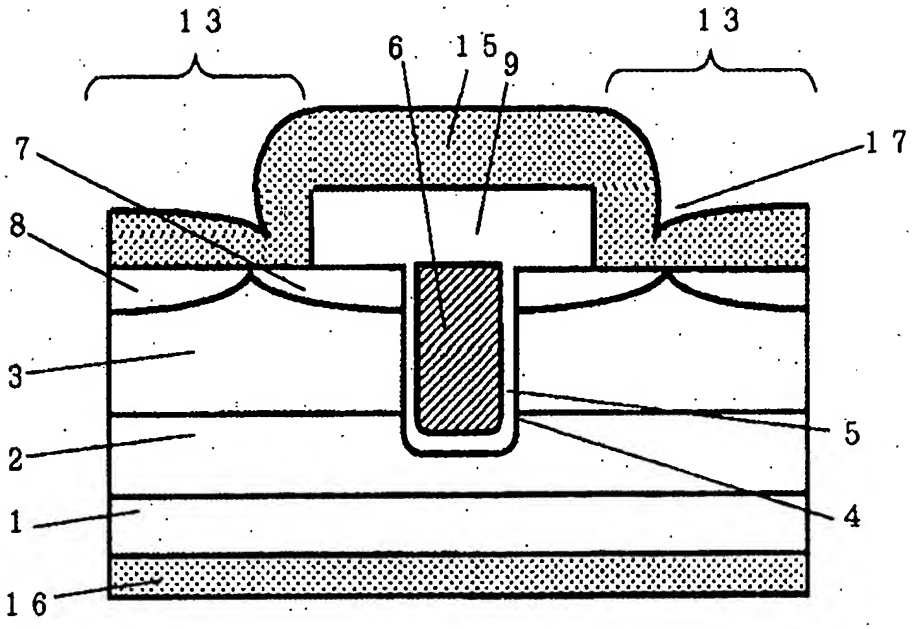
FIG. 1



TD
5/11/06

Replacement Sheet

FIG. 2 Prior Art



TD
5/11/06

FIG. 4

TD
5/11/06

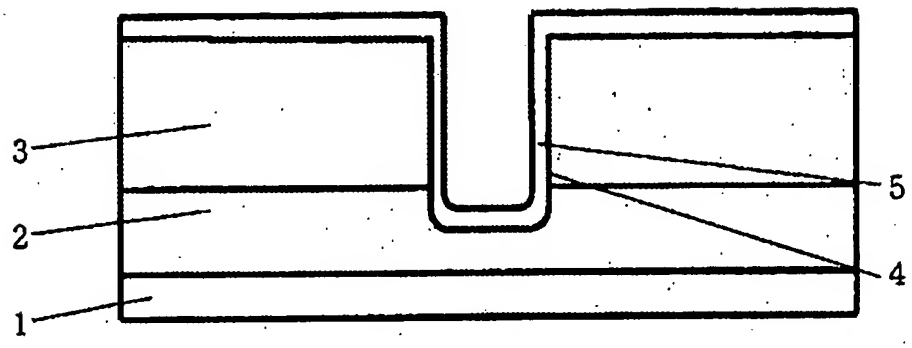


FIG. 5

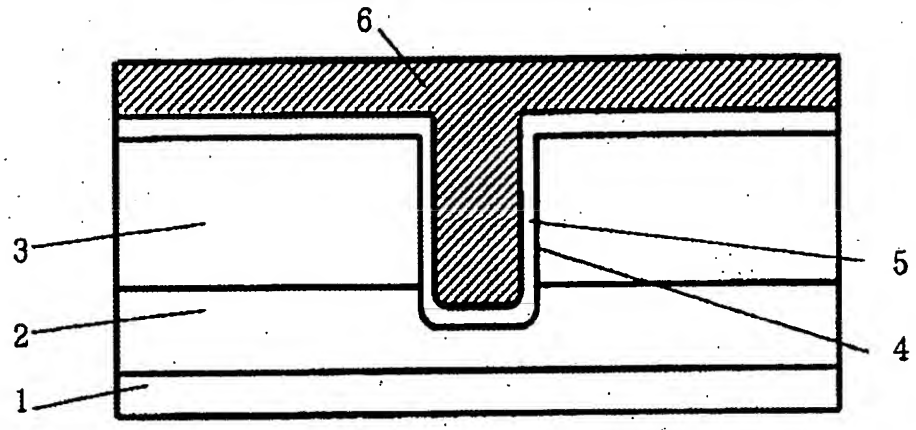
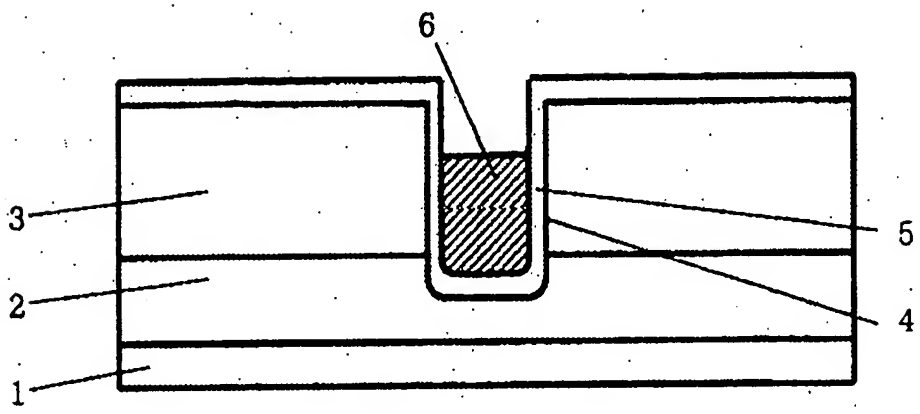
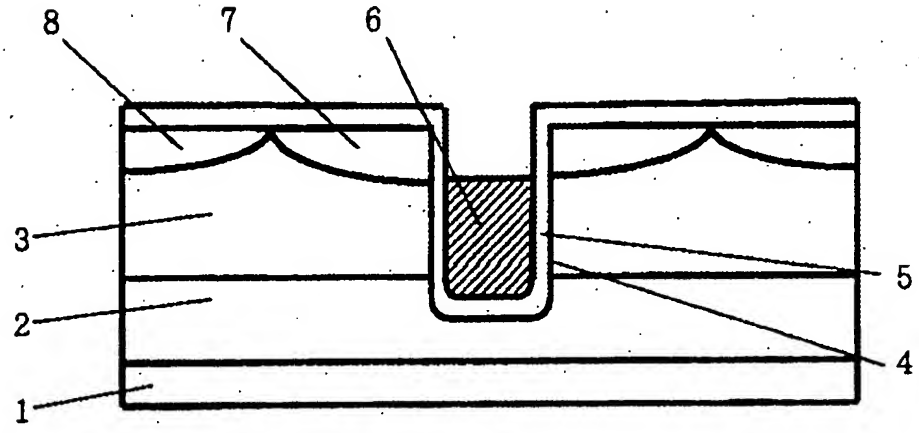


FIG. 6



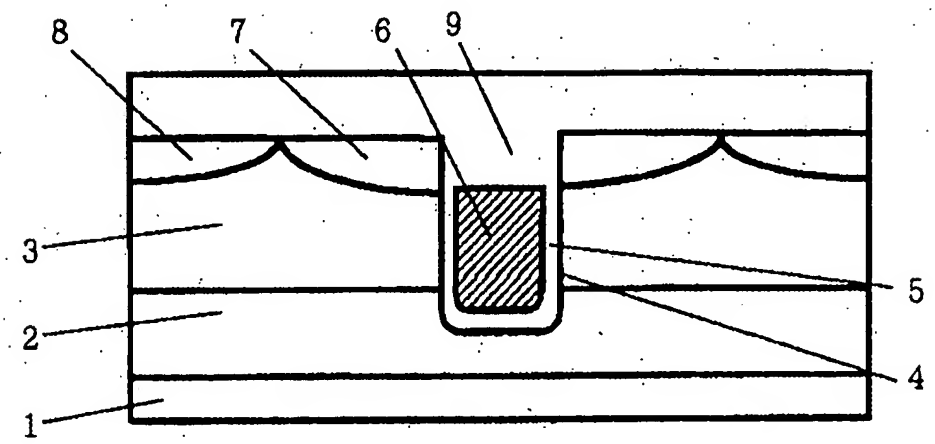
Replacement Sheet

FIG. 7



Replacement Sheet

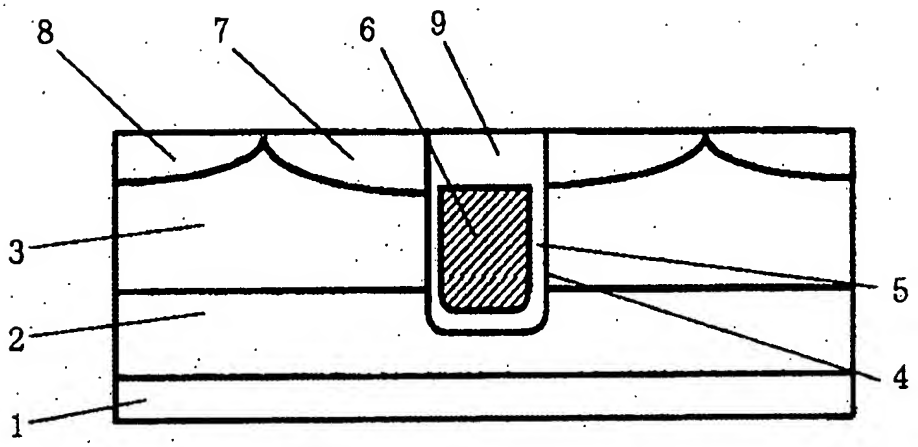
FIG. 8



TJ
5/11/06

Replacement Sheet

FIG. 9



TV
5/11/06

FIG. 10

TV
5/11/06

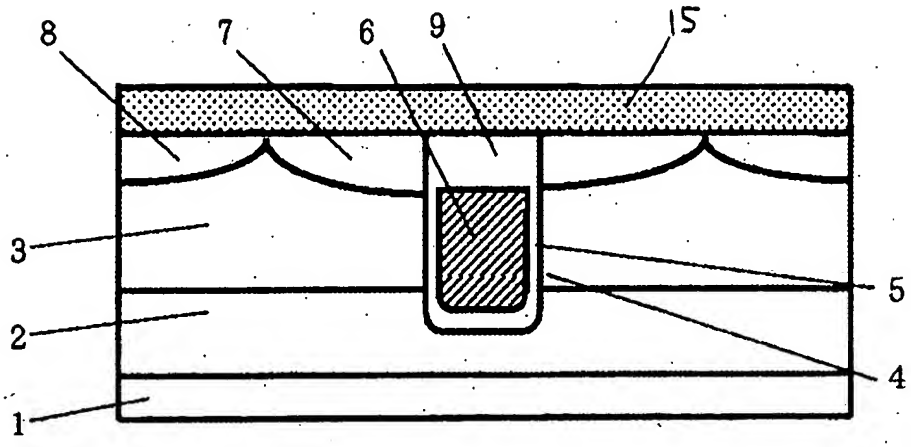
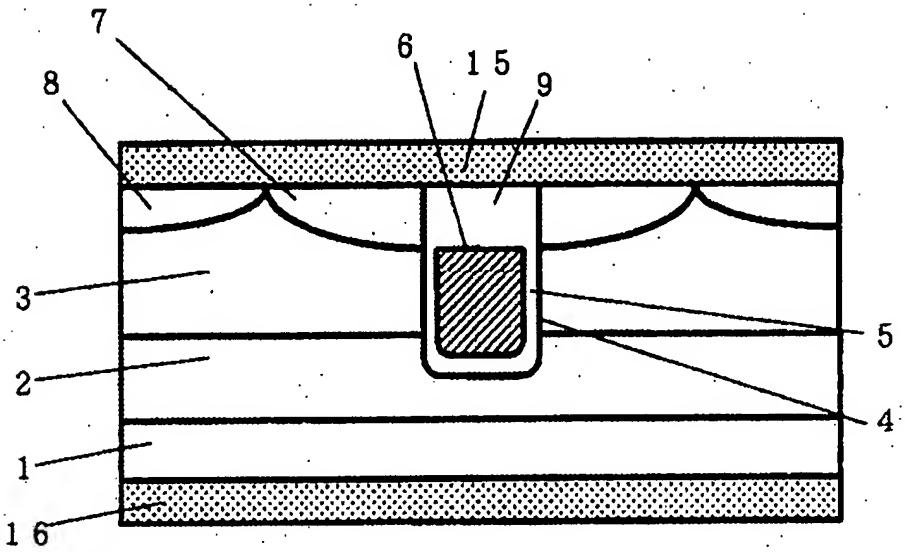


FIG. 11



Replacement Sheet

FIG. 12